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PATENT SPECIFICATION

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(54) A PROCESS FOR ETCHING A SEMICONDUCTOR DEVICE

(71) We, RCA CORPORATION, a corporation organised under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to the manufacture of semiconductor devices having an electrical interconnection pattern in the form of a shaped metallic layer covered by an insulating layer, and more particularly to techniques for selectively etching the overlying insulating layer.

In the manufacture of semiconductor devices in general, and integrated circuits in particular, it is common to provide electrical contacts to and/or interconnections between the various operating regions of the semiconductor element or elements involved, by means of a deposited metallic layer which is etched in accordance with a predetermined pattern.

The presently employed technique of semiconductor manufacture involves the deposition of the metallic layer, usually aluminum, by an evaporation process. The metallic layer is subsequently photoetched by (i) coating the metal with photoresist, (ii) polymerizing selected photoresist regions to render them insoluble in a given developing solution, (iii) subjecting the photoresist coating to the developing solution to remove the unpolymerized regions, and (iv) subjecting the areas of the underlying metallic layer thereby exposed to an etching solution, to which the remaining photoresist material is relatively resistant.

This prior art metal etching process, however, is of limited usefulness wherein it is desired to etch extremely fine line patterns, i.e. patterns having line widths on the order of a few tenths of a mil. At such narrow line widths, undercutting of the metal layer during etching becomes a severe problem. This problem is aggravated by the relatively poor adhesion between the photoresist coating and the underlying metal layer. Presently employed processing techniques include a heat treating step in which the metal layer is baked before the photoresist is applied, in order to improve photoresist adherence. The improvement realized by means of such a baking step, however, is limited, and undercutting of the metal layer during etching still occurs to a considerable extent.

Another problem in the etching of fine resolution patterns is due to the relatively poor resistance offered by the photoresist coating to the solution used to etch the underlying metal layer. As a result, batch process etching is not feasible, since different etching times are required for the processing of semiconductor wafers having metallic layers of varying thickness (it is not practicable to insure absolutely uniform metal layer thickness in a mass production environment). If the entire batch of wafers is immersed in the etching solution for a sufficient time to etch the thickest of the metallic layers, the remaining layers become overetched and experience severe undercutting.

Another problem inherent in the metal etching processes heretofore known lies in the limited sharpness of definition obtainable, due to the graduated thickness of the photoresist layer at the edges thereof.

One approach to the alleviation of these problems has involved the step of, immediately after depositing the metal layer which is to be subsequently etched to provide the desired interconnections, coating the metal layer with a protective insulating layer. The insulating layer is subsequently etched to provide a pattern corresponding to the desired interconnection arrangement, so that the insulating layer may act as an etch mask during the subsequent metal etching operation. Thereafter, another layer of insulating material is deposited to protect the

integrated circuit chip, and etched to expose only the portions of the underlying metallic layer which are to serve as bonding pad areas for external connections to the integrated circuit.

In practicing the step of removing selected portions of the insulating layer to expose the underlying metallic bonding pad areas, it has been found that a number of the metal layer portions comprising the bonding pads are substantially deteriorated or completely destroyed by the etching solution, while the other bonding pads remain relatively unaffected.

Accordingly, it is an object of this invention to provide an improved process for etching an insulating layer to expose underlying metallic bonding pads, without deteriorating the underlying pads.

According to the invention there is provided a semi-conductor device manufacturing process comprising the steps of providing a substrate having a plurality of regions of semiconductor material forming a number of semiconductor elements, each element having at least one contact region adjacent one surface of the substrate; and depositing on said one substrate surface a metallic layer, said layer providing a number of terminal areas electrically coupled to corresponding semiconductor element contact regions, the improvement comprising the steps of; depositing an insulating layer on said metallic layer; and subjecting the portions of said insulating layer overlying said terminal areas to a given etching solution to remove said insulating layer portions without substantially deteriorating the underlying terminal areas, thereby exposing said underlying areas, said etching solution being substantially electrically nonconductive, and comprising hydrofluoric acid, a buffering agent, and an organic substance selected from the group comprising alcohols and carboxylic acids.

In the accompanying drawing:

Figure 1 is a plan view of an integrated circuit having an overlying protective insulating layer thereon;

Figure 2 is a cross-sectional view of one of the bonding pads of the circuit of Figure 1; and

Figures 3 to 9 show, during various intermediate stages of manufacture, a planar diode made according to the invention.

Example

The integrated circuit 20, shown in Figure 1, comprises a die of semiconductor material having a number of deposited aluminum bonding pads 21 peripherally disposed thereon. An array 22 (not shown) of electrically interconnected semiconductor elements is centrally disposed on the wafer. Each of the bonding pads 21 is electrically connected to a different region of an element of the array 22.

The bonding pads 21 and the metallic interconnections of the integrated circuit 20 are provided by means of a deposited aluminum layer 23 (see Figure 2), which makes electrical contact to the various elements of the array 22 through holes in a silicon dioxide insulating layer 24 disposed on the semiconductor surface. A glassy silicon dioxide insulating layer 25 overlies the metallic interconnection layer 23.

In manufacturing the integrated circuit 20, the elements of the array 22 are provided by conventional planar diffusion techniques, utilizing a thermally grown silicon dioxide diffusion mask. The aluminum layer 23 is deposited and subsequently etched to provide the desired interconnection pattern.

In order to protect the relatively thin and soft aluminum metallization layer 23 from scratching or other deterioration, it is desirable to provide the overlying protective glassy insulating layer 25 thereon. The insulating layer 25 is subsequently etched to provide holes 26 therein exposing each of the bonding pads 21, so that external electrical connections can be provided to the integrated circuit 20.

Prior attempts to provide such a structure have, however, been unsuccessful, due to the partial or complete destruction of selected ones of the bonding pads 21 when subjected to the solution used to etch the protective insulating layer 25.

Etching solutions which have previously been employed to remove portions of the glassy insulating layer 25 overlying the bonding pads 21 comprise a mixture of hydrofluoric acid and a suitable buffering agent, such as ammonium fluoride. When the etching solution has removed the desired portion of the insulating layer 25 and contacts the underlying bonding pad 21, an electrochemical or "battery" action is set up between the various bonding pads 21, with consequent electrochemical etching of selected pads, i.e. those pads which are at the highest electrochemical potentials. The high electrical conductivity of the buffered hydrofluoric acid etching solution accelerates this process.

Since the integrated circuit 20 may have slightly varying thicknesses of the glassy insulating layer 25 overlying different bonding pad areas, it is not feasible to terminate the etching process at the precise moment when the bonding pad areas are exposed, since each bonding pad area may be exposed at a somewhat different time.

The differences in electrochemical potential between the various bonding pads 21 arise for the fact that each of the bonding pads is connected to a different part of the integrated circuit, and that different parts

of the circuit are associated with different semiconductor regions separated by one or more P-N junctions, each P-N junction having a particular electrochemical potential associated therewith.

We have found that chemical etching of the glassy insulating layer 25 may be achieved without deteriorating the underlying metallic bonding pads 21, by employing an etchant which is substantially electrically nonconductive. The high resistivity of the etching solution substantially prevents the aforementioned undesirable electrochemical etching action from taking place.

In particular, a nonconductive etching solution which comprises (i) hydrofluoric acid, (ii) a buffering agent such as ammonium fluoride, and (iii) an organic substance capable of absorbing water, such as a carboxylic acid, or an alcohol. Glycol or glycerol has been found to provide good results. Such an etching solution works well with various types of glasses, including borosilicate glass as well as silicon dioxide. This etching solution may be employed with various types of underlying bonding pad metals, such as aluminum, nickel, copper, gold, iron, tantalum, silver, titanium, or various combinations of these metals.

The manufacture of a silicon planar epitaxial diode 30 is commenced by diffusing a P type region 1 into an N type silicon epitaxial layer 2, which has been grown upon an N+ silicon substrate 3, as shown in Figure 3.

The diffusion step is carried out, in accordance with conventional semiconductor process technology, by (i) thermally growing a silicon dioxide layer 4 on the epitaxial layer 2, (ii) photoetching the silicon dioxide layer 4 to uncover a selected region 5 of the semiconductor surface, (iii) depositing a suitable acceptor impurity-containing material, such as borosilicate glass, on the exposed surface of the epitaxial layer 2, and (iv) heating the semiconductor body to diffuse the acceptor impurity material (boron) into the epitaxial layer 2 to form the desired P type region. The diffusion step is usually carried out in an oxidizing atmosphere, so that during the diffusion process a thin thermal oxide skin 6 is formed on the exposed surface of the P type region 1.

Similarly, a suitable dopant is employed to provide an N^+ type contact region 16 in the N type layer 2. Thereafter, the silicon dioxide layers 4 and 6 are photoetched to uncover surface areas of the P type region 1 and of the N type region 2 (i.e., the insert N^+ region 16 thereof), as shown in Figure 4.

The next major process step, as shown in Figure 5, involves evaporation of an aluminum film 7 onto the entire upper surface of the semiconductor wafer. The aluminum film 7 may have a thickness on the order of 1 to 2 microns. Other suitable materials such as electroless nickel in combination with other metals may be utilized instead of aluminum for the metallization layer 7.

Immediately after the aluminum layer 7 is deposited, an additional silicon dioxide layer 8 is pyrolytically deposited on the exposed surface of the aluminum layer 7. The pyrolytic silicon dioxide layer 8 exhibits an extremely good adherence to the underlying aluminum layer 7. The hardness of the silicon dioxide layer 8 protects the relatively soft, thin aluminum layer 7 from scratching or other mechanical damage during subsequent handling steps.

The silicon dioxide layer 8 is deposited from the vapor phase by reacting a mixture of silane (SiH_4), oxygen (O_2) and nitrogen (N_2) as the carrier gas, at a temperature between 280° and 400°C., the temperature range of 350° to 370°C. being preferred. The silicon dioxide layer 8 is deposited to a thickness on the order of 0.3 to 0.4 microns the resulting structure being as shown in Figure 6.

The next process step is to deposit on the exposed surface of the silicon dioxide protective layer 8 a coating 9 of a photopolymerizable material, such as one of the photoresists sold under the trade designations KTFR and KPR by Eastman Kodak Company.

Upon exposure to ultraviolet or other suitable actinic radiation, selected portions of the photopolymerizable coating 9 are polymerized. In the structure shown in Figure 7, it is desired to remove only the area of the metallic layer 7 which overlies the silicon dioxide layer 10. Therefore, the actinic radiation pattern, determined by exposure of the coating 9 through a suitable photomask, is such that the entire photopolymerizable coating 9 overlying the metallic layer 7, except the area overlying the silicon dioxide layer portion 10, is polymerized and rendered insoluble in a suitable developing solution, such as Kodak KMER developer followed by Kodak KPR developer for the aforementioned Kodak KTFR or KPR photoresist.

The exposed coating 9 is then immersed in the aforementioned developing solution to remove the portion overlying the silicon dioxide layer portion 10. During this developing step, the silicon dioxide film 8 protects the overlying metal layer 7 from any deterioration during the developing process.

After development, the polymerized photoresist layer 9 is employed as an etching mask to form a hole 11 in the silicon dioxide layer 8, by means of a (substantially electrically nonconductive) buffered hydrofluoric acid etch comprising 5.75 lbs. of 40% (by weight) aqueous ammonium fluoride solution, 1.0

lbs. of 49.3% (by weight) aqueous hydrofluoric acid solution and 1.4 liters of 100% glacial acetic acid.

After the buffered etch has formed the hole 11, the semiconductor wafer is removed from the etching solution. It is not desirable to remove the portion of the metal layer 7 exposed by the hole 11 with a conventional electrically conductive buffered etch solution, since severe undercutting may occur. At this state in the manufacturing process, the semiconductor device structure appears as shown in Figure 7.

After rinsing in dionized water, the semiconductor wafer is immersed in an etching solution comprising a mixture of nitric and phosphoric acids, such as that marketed by Nitine, Inc., Whippany, New Jersey. This etching solution, which is maintained at a temperature of the order of 40° to 43°C., removes the portion of the metal layer 7 exposed by the hole 11, but has substantially no effect on the silicon dioxide layer 8, which is chemically resistant to the nitric/phosphoric acid etching solution. If desired, the photoresist coating 9 may be removed by immersion in a stripping solution marketed under the designation J-100 by Industrial-Richem Labs., Texas, prior to the metal layer etching step. The silicon dioxide layer 8, being chemically resistant to the etch used to remove the photoresist coating 9, also protects the underlying portions of the metallic layer 7 during the photoresist removal step.

The aforementioned nitric/phosphoric acid aluminum etching solution has been found to etch through a 1.6 micron thickness of aluminum in approximately 5 minutes. The silicon dioxide layer 8, which serves as an etch mask, adheres extremely well to the metal layer 7, so that undercutting is substantially eliminated. The use of the silicon dioxide layer 8 as an etch mask permits a number of semiconductor wafers, having varying thicknesses of the metallic layer 7, to be etched in a single batch process operation.

The portions of the aluminum layer 7 in contact with the exposed surface of the P type region 1 and the N^+ type contact region 16 are "alloyed" to the semiconductor surface, in order to provide good ohmic contact thereto, by heating the semiconductor wafer at a temperature of the order of 530° to 550°C. for a time on the order of 16 minutes.

After removal of the photoresist coating 9 and alloying of the aluminum layer 7, a fresh silicon dioxide film 12, (see Figure 8) is pyrolytically deposited on the entire upper surface of the semiconductor wafer. This silicon dioxide film may be deposited by vapor phase reaction of silane and oxygen, as previously described, to a thickness on the order of 0.7 microns.

A fresh photoresist coating 13 is then applied to the exposed surface of the silicon dioxide film 12. The photoresist coating 13, which may comprise Kodak KTFR or KPR photopolymerizable material, is then exposed and developed to serve as an etch mask for providing apertures (using the aforementioned buffered hydrofluoric acid etch) in the silicon dioxide layers 8 and 12, so that suitable electrodes may be provided in the silicon dioxide layer apertures. The semiconductor device, after deposition of the photoresist coating 13, is as shown in Figure 8.

After the (nonconductive) buffered hydrofluoric acid etch removes the desired portions of the silicon dioxide layers 12 and 8 to expose the underlaying parts of the aluminum layer 7 which are to serve as the diode bonding areas, it is found that substantially no deterioration of these bonding areas occurs due to immersion in the etching solution. While etching of the silicon dioxide layers 12 and 8 usually takes 3 to 5 minutes, we have observed no substantial deterioration of the underlying bonding pad areas even when immersed in the buffered etching solution for periods of time as long as 10 minutes.

After the photoresist coating 13 has been employed as an etching mask to provide apertures in the regions 14 and 15 of the silicon dioxide layers 8 and 12, the remaining photoresist is moved in the manner previously described, and the wafer is cleaned and rinsed. Terminal leads (not shown) may then be ultrasonically bonded to the aluminum pads exposed by each of the apertures 14 and 15.

The resulting silicon planar epitaxial diode is as shown in Figure 9. The silicon dioxide layer 8 serves to protect the underlying aluminum layer 7 from chemical and mechanical deterioration during virtually all processing steps after evaporation of the aluminum layer.

WHAT WE CLAIM IS:—

1. A semiconductor device manufacturing process comprising the steps of providing a substrate having a plurality of regions of semiconductor material forming a number of semiconductor elements, each element having at least one contact region adjacent one surface of the substrate; and depositing on said one substrate surface a metallic layer, said layer providing a number of terminal areas electrically coupled to corresponding semiconductor element contact regions, the improvement comprising the steps of depositing an insulating layer on said metallic layer; and subjecting the portions of said insulating layer overlying said terminal areas to a given

etching solution to remove said insulating layer portions without substantially deteriorating the underlying terminal areas, thereby exposing said underlying areas, said etching solution being substantially electrically nonconductive, and comprising hydrofluoric acid, a buffering agent, and an organic substance selected from the group comprising alcohols and carboxylic acids.

2. A process as claimed in claim 1, wherein said insulating layer is glassy, and said etching solution comprises hydrofluoric acid, a buffering agent, and a carboxylic acid.

3. A process as claimed in claim 2, wherein said buffering agent comprises ammonium fluoride and said carboxylic acid comprises glacial acetic acid.

4. A process as claimed in claim 3, wherein said solution comprises the following ingredients in the indicated relative proportions: 1.0 lb. 49.3% (by weight) aqueous hydrofluoric acid solution: 5.75 lb. 40% (by weight) aqueous ammonium fluoride solution: and 1.4 liter 100% glacial acetic acid.

5. A process as claimed in claim 1, wherein said insulating layer comprises silicon dioxide and said metallic layer comprises aluminum.

6. A semiconductor device fabricated substantially as described with reference to Figures 1-9 of the accompanying drawing.

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1228083 COMPLETE SPECIFICATION
1 SHEET

This drawing is a reproduction of the Original on a reduced scale

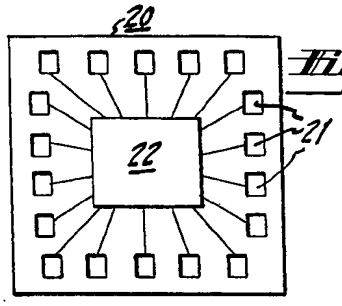

Fig. 1.

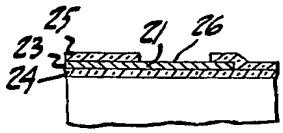

Fig. 2.

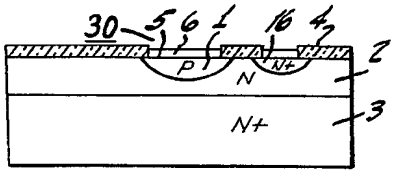

Fig. 3.

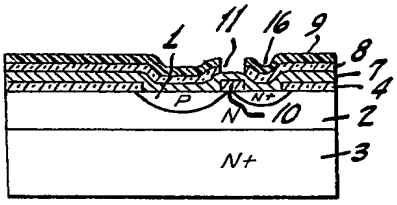

Fig. 7.

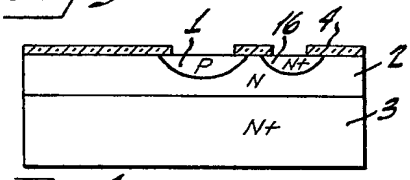

Fig. 4.

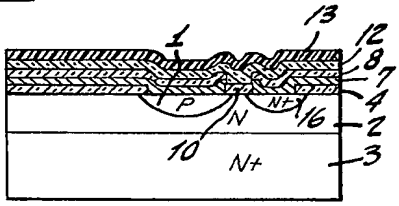

Fig. 8.

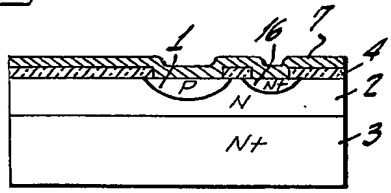

Fig. 5.

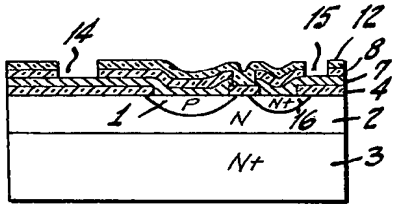

Fig. 9.

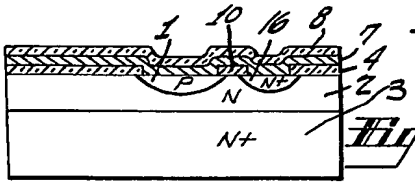

Fig. 6.